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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,774	03/06/2002	Sumio Morioka	JP920010005US1	8926

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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,774	MORIOKA ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because the prior art label should be removed from figures 6, 10-13 and 15-20, as these figures are for the present invention as per specification pages 16-17. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 4, 5, 7, 8, 10, 11, 13, 14, 15, 16, 17, 18, 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Riggle et al. (US 5,107,503).

Riggle et al. anticipate claim 1.

Riggle et al. teach a combinational circuit comprising: a plurality of multipliers, independently performing two or more multiplications for coded digital signals in a Galois extension field GF(2.sup.m), where m is

an integer equal to or greater than 2, wherein said multipliers include an input side XOR calculator, an AND calculator, and an output side XOR calculator, and wherein said multipliers share said input side XOR calculator (abstract, col. 8, lines 4-5, col. 9 lines 6-29, col. 23, line 66-col. 24, line 12, Riggle et al.).

- Riggle et al. anticipate claim 2.

Riggle et al. teach the combinational circuit, wherein the input of the multipliers is commonly used (figure 16, 17, col. 18, lines 56-66, Riggle et al.).

- Riggle et al. anticipate claim 4.

Riggle et al. teach the combinational circuit, wherein syndromes obtained by said coded digital signal are input (figure 1, col. 6, lines 47-56, Riggle et al.).

- Riggle et al. anticipate claim 5.

Riggle et al. teach the combinational circuit that is used for at least one of decoding, error correction and encryption (figure 1, col. 5, lines 54-56, Riggle et al.).

- Riggle et al. anticipate claim 7.

Riggle et al. teach a combinational circuit for performing a logical sum calculation for a Galois extension field GF(2.sup.m), where m is an integer equal to or greater than 2, comprising: a plurality of multipliers, each of which includes an adder connected between an AND calculator and an output side XOR calculator, wherein said output side XOR calculator is used in common, and wherein outputs of said AND calculators in said multipliers are added by said adders, and addition results are calculated by said output side XOR calculator that is used in common (figure 3, 4, 10, 13, 23, col. 11, lines 8-25, col. 15, lines 15-23, col. 21, line 34-col. 22, line 5, Riggle et al.).

- Riggle et al. anticipate claim 8.

Riggle et al. teach the combinational circuit, wherein said multipliers have an input that is commonly used, and said input side XOR calculator is used in common by said multipliers (figure 16, 17, col. 18, lines 56-66, Riggle et al.).

- Riggle et al. anticipate claim 10.

Riggle et al. teach the combinational circuit, wherein syndromes obtained by said coded digital signal are input (figure 1, col. 6, lines 47-56, Riggle et al.).

- Riggle et al. anticipate claim 11.

Riggle et al. teach the combinational circuit that is used for at least one of decoding, error correction and encryption (figure 1, col. 5, lines 54-56, Riggle et al.).

- Riggle et al. anticipate claim 13.

Riggle et al. teach an encoder including the combinational circuit (col. 5, lines 65-67, Riggle et al.).

- Riggle et al. anticipate claim 14.

Riggle et al. teach a decoder including the combinational circuit (col. 4, lines 3-7, Riggle et al.).

- Riggle et al. anticipate claim 15.

Riggle et al. teach a semiconductor device used for processing a digital signal (figure 1, col. 5, lines 54-57, col. 7, line 62, Riggle et al.), said device comprising: input means, for receiving a coded digital signal (col. 6, lines 25-35, Riggle et al.); processing means, for processing said coded digital signal and for calculating coefficients of error locator polynomial and coefficients of error value polynomial (col. 15, lines 10-26, Riggle et al.); and output means, for outputting a digital signal obtained by correcting errors using said coefficients of error locator polynomial and said coefficients of error value polynomial (col. 4, lines 7-9, Riggle et al.), wherein said input means is constituted by a sequential circuit (figure 1, col. 7, lines 23-30, Riggle et al.), and said processing means is constituted by a combinational circuit (col. 22, lines 57-61, Riggle et al.).

- Riggle et al. anticipate claim 16.

Riggle et al. teach the semiconductor device, wherein said combinational circuit includes: a plurality of multipliers, independently performing two or more multiplications for coded digital signals in a Galois extension field GF(2.sup.m), where m is an integer equal to or greater than 2, wherein said multipliers include an input side XOR calculator, an AND calculator, and an output side XOR calculator, and wherein said multipliers share said input side XOR calculator (abstract, col. 8, lines 4-5, col. 9 lines 6-29, col. 23, line 66-col. 24, line 12, Riggle et al.).

- Riggle et al. anticipate claim 17.

Riggle et al. teach the semiconductor device, wherein said combinational circuit includes: a logical sum calculator for a Galois extension field GF(2.sup.m), where m is an integer equal to or greater than 2,

wherein said multipliers include an adder connected between said AND calculator and said output side XOR calculator, wherein said output side XOR calculator is used in common, and wherein outputs of said AND calculators in said multipliers are added by said adders, and addition results are calculated by said output side XOR calculator that is used in common (figure 3, 4, 10, 13, 23, col. 11, lines 8-25, col. 15, lines 15-23, col. 21, line 34-col. 22, line 5, Riggle et al.).

- Riggle et al. anticipate claim 18.

Riggle et al. teach the semiconductor device, wherein said multipliers have commonly used input, and said input side XOR calculator is used in common by said multipliers (figure 16, 17, col. 18, lines 56-66, Riggle et al.).

- Riggle et al. anticipate claim 20.

Riggle et al. teach the semiconductor device that is used for at least one of decoding, error correction and encryption (figure 1, col. 5, lines 54-56, Riggle et al.).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 3, 9, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riggle et al. (US 5,107,503) as applied to claims 1, 7 and 15 above, and further in view of Sugawara (US 6,718,138 B1).

As per claim 3, Riggle et al. substantially teach the claimed invention described in claim 1 (as rejected above). Riggle et al. also teach an error location calculator that calculates an error location for a digital signal, and an error value calculator (col. 6, lines 49-56, Riggle et al.).

However Riggle et al. do not explicitly teach the specific use of a digital signal transmitted using wavelength division multiplexing.

Sugawara in an analogous art teaches a transmission quality monitoring apparatus for monitoring transmission qualities of n-value digital signals (n being a natural number equal to or larger than 2) in a plurality of wavelength channels, which are optically transmitted over an optical transmission line of a wavelength division multiplexing network, comprising optical branching means for branching a part of transmitted light from the optical transmission line of the wavelength division multiplexing network (col. 4, lines 15-20, Sugawara).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Riggle et al.'s patent with the teachings of Sugawara by including an additional step of using a digital signal transmitted using wavelength division multiplexing.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a digital signal transmitted using wavelength division multiplexing would provide the opportunity to provide different transmission speeds, transmission frame formats and modulation systems for different wavelength channels.

- As per claim 9, Riggle et al. and Sugawara teach the additional limitations.

Riggle et al. teach an error location calculator that calculates an error location for a digital signal, and an error value calculator (col. 6, lines 49-56, Riggle et al.).

Sugawara teaches a digital signal transmitted using wavelength division multiplexing (col. 4, lines 15-20, Sugawara).

- As per claim 19, Riggle et al. and Sugawara teach the additional limitations.

Riggle et al. teach the semiconductor device, wherein said combinational circuit is used for an error location calculator, for calculating an error location for a digital signal, and an error value calculator (col. 6, lines 49-56, Riggle et al.).

Sugawara teaches a digital signal transmitted using wavelength division multiplexing (col. 4, lines 15-20, Sugawara).

7. Claims 6, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riggle et al. (US 5,107,503) as applied to claims 1 and 7 above, and further in view of Oowaki et al. (US 6,327,654 B1).

As per claim 6, Riggle et al. substantially teach the claimed invention described in claim 1 (as rejected above).

However Riggle et al. do not explicitly teach the specific use of the combinational circuit that is used for a coding circuit and a decoding circuit for cryptography.

Oowaki et al. in an analogous art teach executing circuit configuration by the coding chip based on configuration information to identify an algorithm in randomizing process, and then executing coding process by the coding chip by using the circuit configuration (col. 5, lines 4-8, Oowaki et al.); executing the circuit configuration by the decoding chip based on the configuration information, and then executing decoding process by the decoding chip by using the circuit configuration; and outputting a decoded text by the decoding chip. According to this method, if the randomizing process can be performed variably by using the configuration information, the encryption algorithm can be varied to thus improve the security protection performance (col. 5, lines 14-22, Oowaki et al.). Oowaki et al. teach that the security protection performance of the cryptography can be improved by alternating an encryption algorithm since a circuit configuration in the randomizing process can be varied (col. 6, lines 47-50, Oowaki et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Riggle et al.'s patent with the teachings of Oowaki et al. by including an additional step of using the combinational circuit, that is used for a coding circuit and a decoding circuit for cryptography. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the combinational circuit,

that is used for a coding circuit and a decoding circuit for cryptography would provide the opportunity to improve a security protection performance of cryptography.

- As per claim 12, Riggle et al. and Oowaki et al. teach the additional limitations.

Oowaki et al. teach the combinational circuit that is used for a coding circuit and a decoding circuit for cryptography (col. 5, lines 4-8, lines 14-22, col. 6, lines 47-50, Oowaki et al.).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

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PRIMARY EXAMINER